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```
1464         std::uint32_t perf_tsc_size : 2;
1465         std::uint32_t reserved_2 : 14;
1466         } & narrow_cast<std::uint32_t>(reg[eca]);
1467         machine_core_mask_width = c_apic_id_size;
1468         break;
1469     default:
1470         break;
1471     }
1472 });
1473
1474 switch(machine_vendor & vendor_type == any_silicon) {
1475     case vendor_type::intel:
1476         // see the utterly miserable source code at https://software.intel.com/en-us/articles/intel-9s-architecture-processor-topology-enumeration
1477         for(const std::uint32_t id : machine_x2_apic_ids) {
1478             const full_apic_id_t split = split_apic_id(id, machine_smt_mask_width, machine_core_mask_width);
1479             logical_core_t core = { id, split_smt_id, split_core_id, split_package_id };
1480             for(const cache_t& cache : machine_all_caches) {
1481                 core.shared_cache_ids.push_back(id & cache.sharing_mask);
1482                 core.non_shared_cache_ids.push_back(id & ~cache.sharing_mask);
1483             }
1484             machine_all_cores.push_back(core);
1485             machine_packages[split_package_id].physical_cores[split_core_id].logical_cores[split_smt_id] = core;
1486             for(std::size_t i = 0; i < machine_all_caches.size(); ++i) {
1487                 cache_t& cache = machine_all_caches[i];
1488                 for(const logical_core_t& core : machine_all_cores) {
1489                     cache_instances[core.non_shared_cache_ids].sharing_ids.push_back(core.full_apic_id);
1490                 }
1491             }
1492             break;
1493     case vendor_type::amd:
1494         // paper https://www.amd.com/en-us/resources/white-papers-and-guides/white-papers/amd-processor-topology-enumeration
1495         for(const std::uint32_t id : machine_x2_apic_ids) {
1496             const full_apic_id_t split = split_apic_id(id, machine_smt_mask_width, machine_core_mask_width);
1497             logical_core_t core = { id, split_smt_id, split_core_id, split_package_id };
1498             machine_all_cores.push_back(core);
1499             machine_packages[split_package_id].physical_cores[split_core_id].logical_cores[split_smt_id] = core;
1500             for(std::size_t i = 0; i < machine_all_caches.size(); ++i) {
1501                 cache_t& cache = machine_all_caches[i];
1502                 for(std::size_t j = 0; j < machine_all_cores.size(); ++j) {
1503                     cache_instances[cache.narrow_cast<std::uint32_t>(j) / (cache.sharing_mask + 1_u32)].sharing_ids.push_back(machine_all_cores[j].full_apic_id);
1504                 }
1505             }
1506             break;
1507     default:
1508         break;
1509 }
1510 return machine;
1511 }
1512
1513 void print_topology(fet::memory_buffer& out, const system_t& machine) {
1514     const std::uint32_t total_addressable_cores = get_narrow_cast<std::uint32_t>(machine.all_cores.size());
1515     std::multimap<std::uint32_t, std::string> cache_output;
```

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